REMARKS/ARGUMENTS

Claim Rejections – 35 USC 103

Claims 49 and 60 are rejected under 35 U.S.C. 103(a) as being unpatentable over Miyashita (U.S. Patent No. 5,627,813) in view of Udagawa (Publication No. U.S. 2004/0013065 A1).

Response:

Claim 49

Examiner stated that the combined teaching of Miyashita and Udagawa could disclose all of the claimed features as recited in claim 49. The applicant respectfully disagrees and points out that teachings of the cited prior art are misinterpreted by Examiner.

In col. 14, lines 4-11, Miyashita explicitly states: "Since the control becomes complicated with addition of the calibration function, preferred control is on by digital signal processing using CPU. The CPU 28 has the functions of the comparators 6 to 8 for comparing the laser power monitor voltage with the respective reference voltages, the functions of the U/D counters 9 to 11 for performing up or down counting, and the function of the timing signal generator 20". Therefore, the implementation of the CPU (28) shown in Miyashita Fig. 9 is to **replace** the combination of the comparators (6, 7, 8), the U/D counters (9, 10, 11), and the timing signal generator (20) shown in Miyashita Fig. 1. In other words, as the CPU (28) is a substitute of the combination of the comparators (6, 7, 8), the U/D counters (9, 10, 11), and the timing signal generator (20), the CPU (28) and the combination of the comparators (6, 7, 8) and the U/D counters (9, 10, 11) **do not coexist** in an optical disc apparatus according to teachings of Miyashita. However, Examiner stated that the **CPU (28)** taught by Miyashita could read on applicant's microprocessor, and the combination of the **comparators (6, 7, 8)**, the **U/D counters (9, 10, 11)**, and D/A converters (12, 13, 14) can read on applicant's signal calibration circuit. Such an interpretation of Miyashita's teachings is illogical.

Examiner further stated that comparators (6, 7, 8) taught by Miyashita could perform the claimed operation of determining a power relationship. However, Miyashita's comparator merely compares the laser power monitor signal (V_{mon}) with a reference voltage (V_{ref}) to

determine whether or not the laser power monitor signal (V_{mon}) is equal to the reference voltage (V_{ref}). In other words, Miyashita's comparator is unable to determine a power relationship of values of the laser diode drive signal and the emitted powers of the laser diode. The applicant therefore points out that comparing a power indication signal (i.e., the laser power monitor signal V_{mon}) with a predetermined reference signal (i.e., the predetermined voltage V_{ref}) as taught by Miyashita fails to read on the claimed feature of determining a power relationship relating **values of the drive signal** to **powers of the light emitting device** according to the power indication signal for each of the values of the drive signal. In short, neither the CPU (28) having the comparator functionality nor the comparator (6, 7, 8) taught by Miyashita determines a power relationship relating values of the drive signal to powers of the light emitting device as recited in applicant's claim 49.

Examiner also stated that the photosensor (4) taught by Miyashita can read on the claimed light detector, and the error signal in the comparator (6, 7, 8) taught by Miyashita can read on the claimed analog signal generated from the light detector. However, as clearly shown in Fig. 1 and described in pertinent description in the specification of Miyashita's disclosure, the error signal is generated by the comparator (6, 7, 8) performing a comparison upon the laser power monitor signal (V_{mon}) and the reference voltage (V_{ref}), rather than generated from the photosensor (4) detecting the light emitted from the laser diode (18, 19). The applicant therefore contends that the error signal in the comparator (6, 7, 8) taught by Miyashita fails to read on the claimed analog signal that is defined to be generated from the claimed light detector by detecting the emitted light from the light emitting device.

Examiner also stated that the combination of Miyashita's comparators (6, 7, 8), U/D counters (9, 10, 11) and D/A converters (12, 13, 14) could generate the power indication signal (V_{mon}) according to the analog signal (error signal) and the predetermined reference voltage (V_{ref}). However, as clearly shown in Fig. 1 and described in pertinent description in the specification of Miyashita's disclosure, the error signal is generated by comparing the laser power monitor signal (V_{mon}) with the reference voltage (V_{ref}). Therefore, the power indication signal (V_{mon}) is by no means generated according to the analog signal (error signal)

and the predetermined reference voltage (V_{ref}). That is, based on teachings of Miyashita, the predetermined reference voltage (V_{ref}) would never be involved in generating the laser power monitor signal (V_{mon}). The applicant asserts that the combination of Miyashita's comparators (6, 7, 8), U/D counters (9, 10, 11) and D/A converters (12, 13, 14) fails to read on the claimed signal calibration circuit configured to generate the power indication signal according to the analog signal and the predetermined reference voltage. Similarly, as the CPU (28) shown in Miyashita Fig. 9 has the functions of the combination of the comparators (6, 7, 8), the U/D counters (9, 10, 11), and the timing signal generator (20) shown in Miyashita Fig. 1, the CPU (28) taught by Miyashita also fails to read on the claimed signal calibration circuit configured to generate the power indication signal according to the analog signal and the predetermined reference voltage.

As stated above, Miyashita fails to teach the claimed feature of determining a power relationship relating values of the drive signal to powers of the light emitting device according to the power indication signal for each of the values of the drive signal. Since the claimed power relationship is not taught by Miyashita, the applicant therefore asserts that the Miyashita's device modified to have a non-volatile memory as taught by Udagawa still fails to teach or suggest the claimed non-volatile memory **storing the power relationship** determined by the microprocessor during the calibration mode.

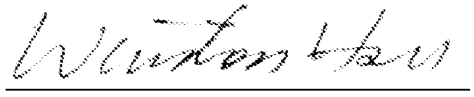
In light of at least above reasons, the applicant asserts that claim 49 should be found allowable over the cited prior art. Withdrawal of rejection and reconsideration of claim 49 are respectfully requested.

Claim 60

Claim 60 is a method claim containing similar limitations recited in claim 49 being an apparatus claim. In view of above arguments of claim 49, the applicant asserts that claim 60 should be found allowable over the cited prior art. Withdrawal of the rejection and reconsideration of claim 60 is respectfully requested.

Applicant respectfully requests that a timely Notice of Allowance be issued in this case.

Sincerely yours,



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